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# Immunity IME

***Inline Memory Encryption IP Core***

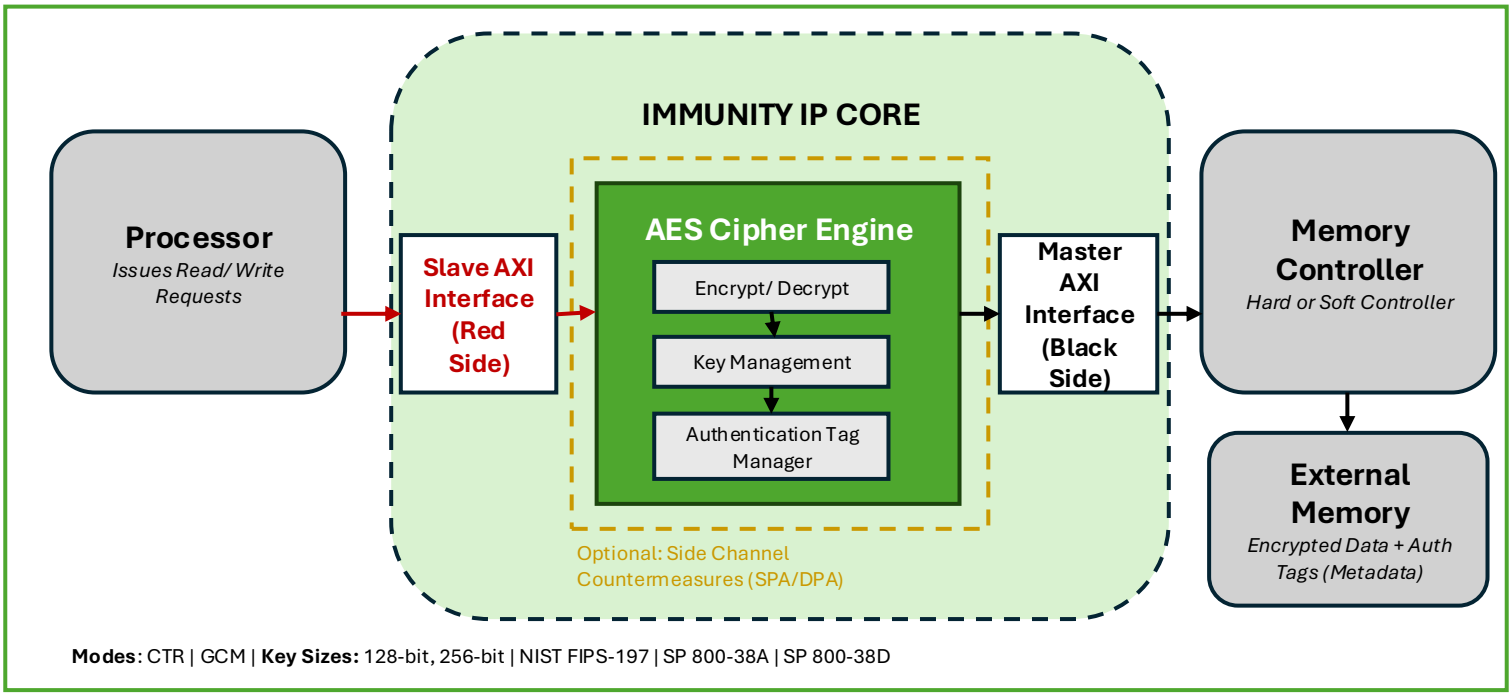
## Overview

The Immunity™ IME IP Core is an inline memory encryption that protects the **confidentiality and integrity of instructions and data stored in external memory**. By inserting Immunity-IME between a processor and memory controller, engineers gain just-in-time encryption, decryption, and authentication for all memory read and write operations– with no changes required to processor firmware or memory controller configuration.

Immunity IME acts as a transparent intermediary:

- Accepts unencrypted ('Red') read/write requests from the processor via its slave AXI interface
- Returns encrypted ('Black') requests via its master AXI interface
- Stores authentication tags ('Metadata') alongside encrypted data in external memory

This approach ensures that data at rest in external memory is always encrypted and authenticated, protecting against both passive interception and active tampering.




**Modes**: CTR | GCM | **Key Sizes:** 128-bit, 256-bit | NIST FIPS-197 | SP 800-38A | SP 800-38D


Contact Idaho Scientific for more information

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## Benefits

| Benefit | Description |
|---|---|
| **Low Risk** | Used in FPGAs on Defense Programs. NIST-approved with proven side channel resistance. |
| **Simple to Integrate** | Drag-and-drop design delivered with reference designs and test benches using common interface IP. |
| **Set and Forget** | No annual maintenance contracts. Implementation of future updates is optional. |
| **Trusted US DoW Supplier** | Developed and supported by cleared US engineers who answer emails, take phone calls, and can travel to ensure smooth integration. |

## Features

| Feature | Detail |
|---|---|
| **Encryption/ Decryption/ Authentication** | AES CTR or GCM cipher, NIST SP 800-38A and SP 800-38D |
| **Standards Compliance** | NIST FIPS-197 |
| **Key Sizes** | 128-bit or 256-bit AES keys |
| **Key Management** | Complete internal key management, NIST 800-133 compliant key generation |
| **Interface** | Compatible with AMBA AXI4- slave (Red) and master (Black) interfaces |
| **Memory Controller Compatibility** | Supports hard or soft memory controllers in Xilinx FPGA and SoC devices |
| **Authentication** | Stores authentication tags (Metadata) alongside encrypted data in external memory |
| **Side Channel Countermeasures** | Optional robust SPA/ DPA countermeasures |

## Deliverables

- Xilinx IP_XACT Package
- Product Documentation
- Example Designs
- Simulation Testbench
- Technical Support
- Maintenance Updates

✓ ***Transparent Operation*** ✓ ***Integrity Protected*** ✓ ***Flexible***

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