



Immunity Chip2Chip

Authenticated Encryption IP Core for Xilinx Chip2Chip Links

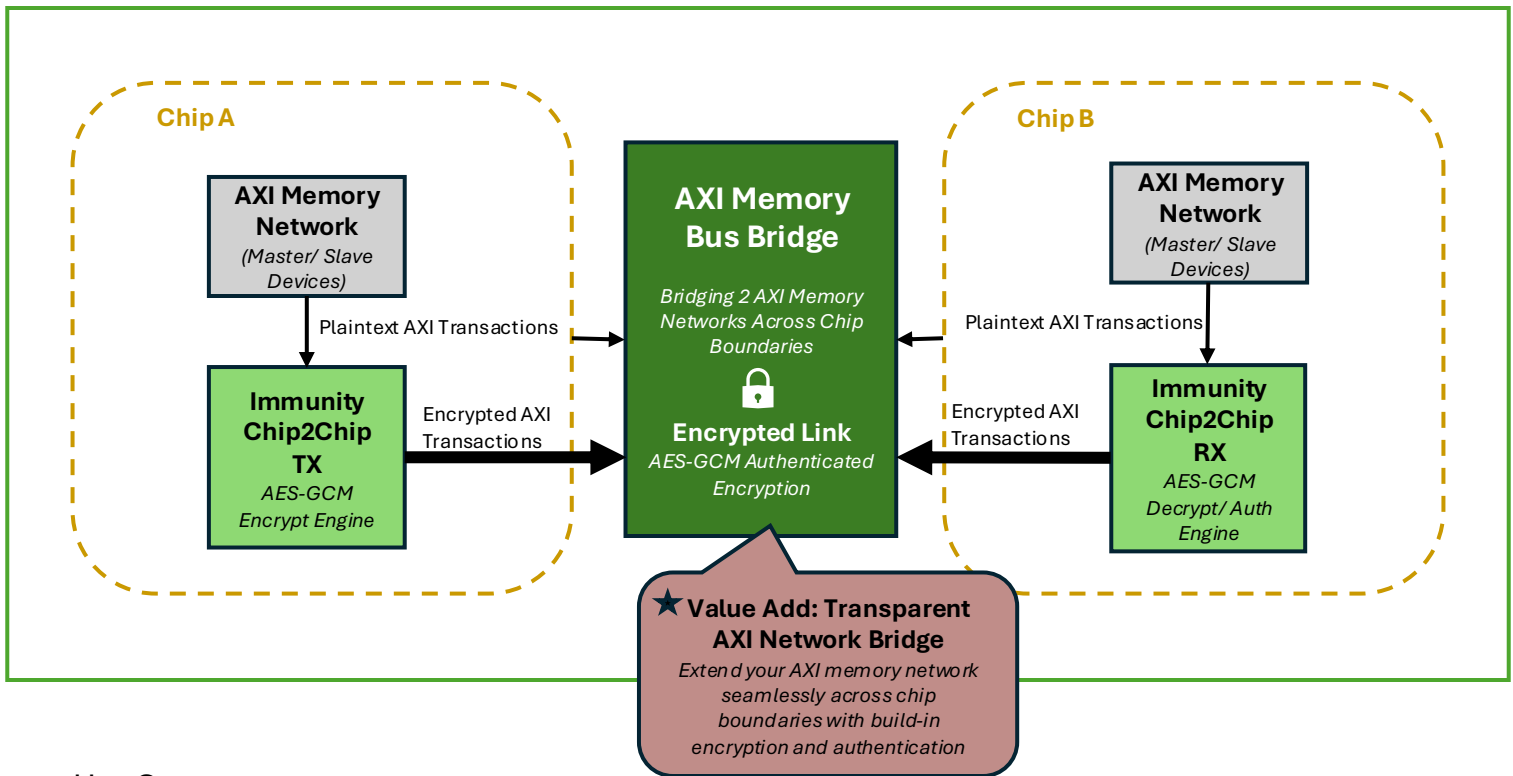
Overview

The Immunity™ Chip2Chip IP Core provides authenticated encryption and decryption to secure Xilinx Chip2Chip communication links. As high-speed chip-to-chip data paths become increasingly vulnerable to interception and tampering, Immunity Chip2Chip delivers AES-GCM-based security with performance optimizations specifically designed to minimize bandwidth and latency impacts.

Immunity Chip2Chip is ideal for multi-FPGA and multi-chip defense systems requiring link-layer confidentiality and integrity without sacrificing throughput.

Immunity Chip2Chip is fully compliant with:

NIST FIPS-197 | NIST SP 800-38D



Use Case

Immunity Chip2Chip is purpose-built for engineers securing high-speed FPGA-to-FPGA or chip-to-chip interconnects in embedded defense systems. It slots directly into existing Xilinx Chip2Chip designs with minimal integration effort through its IP-XACT packaging and AXI4-Lite configuration interface.

Contact Idaho Scientific for more information
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Benefits

Benefit	Description
Low Risk	Used in FPGAs on Defense Programs. NIST-approved with proven side channel resistance.
Simple to Integrate	Drag-and-drop design delivered with reference designs and test benches using common interface IP.
Set and Forget	No annual maintenance contracts. Implementation of future updates is optional.
Trusted US DoW Supplier	Developed and supported by cleared US engineers who answer emails, take phone calls, and can travel to ensure smooth integration.

Features

Feature	Detail
Authentication Encryption	AES-GCM cipher for encryption, decryption, and authentication of Xilinx Chip2Chip links
Performance Optimization	Optimized to minimize bandwidth impacts
Low Latency Design	Cipher buffers designed to minimize latency impacts
Encryption Compliance	NIST FIPS-197
Authentication Compliance	NIST SP 800-38D (GCM)
Configuration Interface	AXI4-Lite interface to configure and enable operation
IP-XACT Package	Easy block design integration and configuration in Xilinx Vivado

Deliverables

Xilinx IP_XACT Package	Hardware Design Project
Bare-Metal Software Project	User API
Technical Support	Maintenance Updates



Purpose-Built



Performance-First



NIST Compliant