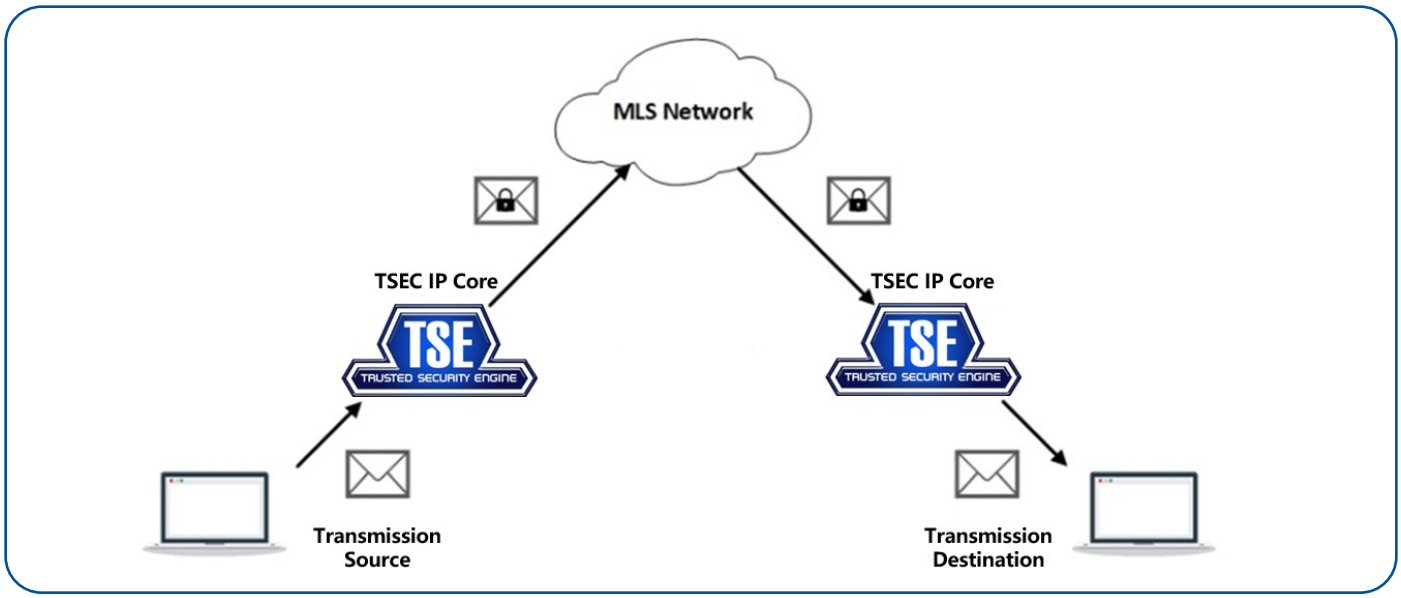
GENERAL DYNAMICS
Mission Systems

TSEC FPGA IP

Supporting hardware enforced security labeling and verification based on NCDSMO "Raise the Bar" design requirements.



The Trusted Security Engine Core (TSEC) is General Dynamics Mission Systems' Field Programmable Gate Array (FPGA) Intellectual Property (IP) solution to support hardware enforced security labeling and verification based on National Cross Domain Strategy and Management Office (NCDSMO) "Raise the Bar" design requirements.

The TSEC IP applies and verifies elements of security and trust to IPv4 Ethernet frames when instantiated in the physical link (or channel) of a network device.

Features

- Hardware enforced domain separation
- Designed for NCDSMO Raise the Bar Compliance
- User programmable separation rulesets
- IPv4 Ethernet frame processing
- Supports 1 or 10 Gb/s operation
- Comprehensive statistics gathering
- Security enforced loopback from egress channel to ingress channels enables secure labelled routing between connected Host Operating System (OS) Devices
- IPv4 address lookups for ingress and egress channels route data to network and/or back to connected Host OS Devices
- Replication of frames destined for multiple connected Host OS Devices

RAISE THE BAR COMPLIANT

TSEC FPGA IP

Overview

The General Dynamics TSEC IP Core enables the development of Multi-Level Security (MLS) communication components that establish and enforce trust within an Ethernet network using an open-standards approach. It also enforces the Security Policy established within an MLS network by performing checks on all Ethernet frames containing IPv4 datagrams at each MLS network endpoint. This validation ensures that packets have not been altered after entry into the MLS network and the destination node contains privilege(s) sufficient to allow delivery of the packet to the MLS device.

This TSEC IP core can be configured to support Single Level (SL) and Multi-Level (ML) domain endpoints. This capability enables standard Ethernet devices to operate securely without requiring an awareness of the MLS Ethernet network implementation details.

Two principal applications for the TSEC IP Core are for use in MLS Switch and MLS Network Interface Card (NIC) devices. A configuration of the TSEC IP Core is available for each of these applications:

- MLS Switch Application – designed for instantiation in a data-channel between two Ethernet Interfaces
- MLS NIC Application – designed for instantiation in a channel between a securely partitioned PCIe host bus and an Ethernet network interface.

Licensing and Ordering Information

For full access to the General Dynamics TSEC IP Core, you must purchase a license through the General Dynamics Open Systems Product Line (OSPL).

For more information about the TSEC core and pricing, visit: **https://gdmissionsystems.com/products/airborne-systems/open-systems-processing**

This product is available for sale to U.S. End-Users only.

TSEC IP Core Facts Table	
Core Specifics	
Supported Device Family	Xilinx Kintex Ultrascale
Supported User Interfaces	Xilinx LocalLink, configuration and statistics
Source Code Format	VHDL
Provided with Product Core	
Design Files	Encrypted RTL
Test Bench	SystemVerilog
Tested Design Flows	
Design Entry	Vivado® Design Suite
Simulation	Questa® Advance Simulator
Synthesis	Vivado® Design Suite
Protocols Supported	
Protocols Supported	IPv4, TCP, UDP, ICMP
Transmission Types Supported	Unicast, Multicast, Broadcast
Network Throughput	1GbE, 10GbE
Support	
Provided by GDMS	

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